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APS Timing Modules

Two VME based modules convert the 352 MHz RF signal from the accelerator to ECL and then distribute these signals to the timing input of the Hydra Control Module. This makes the Hydra modules ideal for fast timing applications such as single pulse triggering.

DTH-R2E converts accelerator signal to ECL.



ECL-1A distributes signals to Control Module

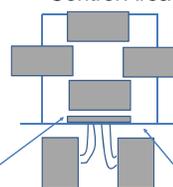
Introduction

Structured around an Altera Cyclone II FPGA, the Hydra trigger electronics are a flexible digital solution for triggering multiple detectors. The architecture developed will trigger up to four detectors, and has additional digital IO lines for external triggering or coordination with additional beam line devices or electronics such as stepper motors or a shutter.

FPGA and timing modules mount in instrumentation rack.

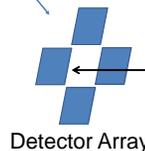


Control Area



Interface module receives detector signals and distributes triggers.

Precise triggering for multiple devices with convenient coordination between control area, detectors, associated instrumentation and the accelerator.



The remotely-mounted interface module receives signals from the detector and passes them to the control module via RS485 communications lines. This inexpensive module could be easily redesigned for communication with various detectors or beamline devices.



Lemo breakouts for convenient monitoring of communications lines.

Hydra Interface Module



Hydra Control Module

Trigger signals and user interface are handled by the Hydra Control Module. This module couples an Altera Cyclone-II FPGA with a μ C5282 microcontroller. The FPGA handles all communications with the detectors, and runs the real-time trigger logic. Easily configurable via Altera's Quartus II software, the FPGA provides a flexible platform which is capable of hosting multiple custom trigger modes, and can even be reconfigured for special experimental conditions.

The microcontroller is an EPICS IOC running the RTEMS real-time OS, which be configured to give users control over parameters within the trigger logic (custom delays for specific devices, etc). Interactions between the FPGA and microcontroller are mediated by the "bus bridge" that was developed here at the APS. Bus bridge allows data transactions and interrupt processing between the controller and FPGA.

For fast timing applications, the timing input allows clocking or triggering on the APS timing signal.

Micro-controller runs EPICS – allowing user control of trigger parameters

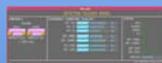


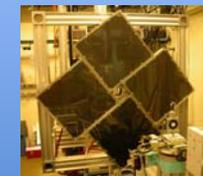
Fig. 4



The electronics have been deployed to trigger the WAXS detector in the Sector 1-IDC. This is a large solid angle instrument composed of four GE amorphous silicon detectors. As designed by GE, three slave detectors were triggered by one master detector. The scheme worked, but the timing was non-uniform, and slave detectors missed ~5% of triggers.

Hydra GE Detector

The new electronics have improved timing synchronization to 2 μ s, simplified the hardware setup, and permit extended running without dropped frames.



Timing resolution is limited by 500 KHz clock on detector interface cards.

